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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/462,994	01/14/2000	UDO SCHWALKE	P99.2666	5747

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EXAMINER
KEBEDE, BROOK

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 05/08/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application No.	Applicant(s)	
	09/462,994	SCHWALKE ET AL.	
	Examiner	Art Unit	
	Brook Kebede	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 February 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *15* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Allowable Subject Matter

1. The indicated allowability of claims 14 and 19 is withdrawn in view of the newly discovered reference(s) to Shimomura et al. (US/5,736,421). Rejections based on the newly cited reference(s) follow.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action::

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 11, 15, 16, 18, and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Hirakawa et al. (US/4,590,508).

Re claim 11, Hirakawa et al. disclose an integrated circuit arrangement having at least one doped region (103-2) is provided in a semiconductor substrate (201); a plane arranged on a surface of the semiconductor substrate (201) having a number of conductive useful structures (104-1 104-2) and at least one conductive filler structure (not labeled) (i.e., a dummy gate or

resistor); and the conductive filler structure (not labeled) is conductively connected to the doped region (103-7) (see Figs. 3(a) - 10).

Re claim 15, as applied to one of the claims 11 above, Hirakawa et al. disclose all the claimed limitation including the limitation wherein the conductive useful structures (104-1 104-2) are gate electrodes; and wherein the conductive filler structure (not labeled) contains the material of the gate electrode (see Figs. 3(a) – 10).

Re claim 16, as applied to one of the claims 11 above, Hirakawa et al. disclose all the claimed limitation including the limitation whereby the doped region (103-7) is a doped well or the semiconductor substrate (10) (see Figs. 3(a) - 10).

Re claim 18, Hirakawa et al. disclose a method for manufacturing an integrated circuit arrangement comprising: forming a doped region (103-7) in a semiconductor substrate (201); forming a plane (not labeled) on a surface of the semiconductor substrate (201) by applying a structuring a conductive useful structures (104-1 104-2) and at least one conductive filler structure (not labeled) producing an insulation layer (207) surrounding and covering the conductive useful structures (104-1 104-2) and the conductive filler structure (not labeled); and producing a conductive connection between the conductive filler structure (not labeled) and the doped region (103-7) (see Figs. 3(a)-10).

Re claim 21, as applied to one of the claims 18 above, Hirakawa et al. disclose all the claimed limitation including the limitation whereby the doped region (103-7) is the semiconductor substrate (201) (see Figs. 3(a) - 10).

5. Claims 11 and 13-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Shimomura et al. (US/5,736,421).

Re claim 11, Shimomura et al. disclose an integrated circuit arrangement having at least one doped region (106) is provided in a semiconductor substrate (101); a plane arranged on a surface of the semiconductor substrate (101) having a number of conductive useful structures (113) and at least one conductive filler structure (112) (i.e., a dummy gate or resistor); and the conductive filler structure (112) is conductively connected to the doped region (106) (see Fig. 1).

Re claim 13, as applied to claim 11 above, Shimomura et al. disclose all the claimed limitation including the limitation a contact (not labeled) connecting the conductive filler structure (112) to the doped region (106) via a via hole (not labeled) (see Fig. 1).

Re claim 14, as applied to claim 13 above, Shimomura et al. disclose all the claimed limitation including the limitation wherein said through hole (not labeled) overlaps said conductive filler structure (112) and said doped region (106) exposing surface of the said conductive filler structure (112) and said a surface of said doped region (106), said contact (not labeled) being in communication with said conductive filler structure (112) and said surface of the doped region (106) (see Fig. 1).

Re claim 15, as applied to one of the claims 11 above, Shimomura et al. disclose all the claimed limitation including the limitation wherein the conductive useful structures (113) are gate electrodes; and wherein the conductive filler structure (112) contains the material of the gate electrode (i.e., polysilicon, see Col. 7, line 61 – Col. 8, line 26) (see Fig. 1).

Re claim 16, as applied to one of the claims 11 above, Shimomura et al. disclose all the claimed limitation including the limitation whereby the doped region (106) is a doped well or the semiconductor substrate (101) (see Fig. 1).

Re claim 17, as applied to on of the claims 16 above, Uehara et al. disclose all the claimed limitation including the limitation a metallization layer (not labeled) is arranged above the plane wherein the conductive filler structure (112) is arranged; and a further contact connecting the conductive filler structure (112) and the metallization layer (not labeled) (see Fig. 1)

Re claim 18, Shimomura et al. disclose a method for manufacturing an integrated circuit arrangement comprising: forming a doped region (106) in a semiconductor substrate (101); forming a plane (not labeled) on a surface of the semiconductor substrate (101) by applying a structuring a conductive useful structures (113) and at least one conductive filler structure (112) producing an insulation layer (106) surrounding and covering the conductive useful structures (113) and the conductive filler structure (112); and producing a conductive connection between the conductive filler structure (112) and the doped region (106) (see Fig. 6-9(e)).

Re claim 19, as applied to claim 18 above, Shimomura et al. disclose all the claimed limitation including the limitation wherein said steps of producing connection between said conductive filler structure (112) and said doped region (106) further comprsing steps of: opening a through hole (not labeled) in said insulation layer (106), said though hole (not labeled) respectively partially overlapping said conductive filler structure (112) and said the doped region (106) for partially uncovering a surface of said doped region (106) and surface of said conductive filler structure (112); and forming a contact (not labeled) through hole (not labeled), said contact (not labeled) being in communication with said surface of said conductive filler structure (112) and said surface of said doped region (106) (see Fig. 1)

Re claim 20, as applied to claim 18 above, Shimomura et al. disclose all the claimed limitations including producing a metallization layer (not labeled) above the plane wherein the conductive filler structure (113) is formed; producing a further contact (not labeled) connecting the conductive filler structure (112) connecting to the metallization layer (not labeled) (see Fig. 1).

Re claim 21, as applied to one of the claims 11 above, Shimomura et al. disclose all the claimed limitation including the limitation whereby the doped region (106) is the semiconductor substrate (101) (see Fig. 1).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shimomura et al. (US/5,736,421) in view of Uehara et al. (US/5,598,902).

Re claim 12, as applied to claim 11 above, Shimomura et al. disclose all the claimed limitation including the limitation a planarizing insulation layer (106) surrounding the conductive useful structures (113) (see Fig. 1).

However, Shimomura et al. do not specifically disclose wherein the conductive useful structures (113) and the conductive filler structure (112) exhibit essentially the same height.

Uehara et al. disclose integrated circuit arrangement having at least one doped region (21) is provided in a semiconductor substrate (10); a plane arranged on a surface of the semiconductor substrate (10) having a number of conductive useful structures (50a) and at least one conductive filler structure (50b); and wherein the conductive useful structures (50a) and the conductive filler structure (50b) exhibit essentially the same height (see Fig. 6). Uehara et al. also disclose that "he lower films of the dummy electrodes (i.e., conductive filler structure) are formed flush with the isolation and in contact with the side edges of the isolation. With the dummy electrodes (i.e., conductive filler structure), any gate electrode (i.e., conductive useful structure) can be formed in a line-and-space pattern (i.e., exhibiting essentially same height), so that the finished sizes of the gate electrode become uniform. This enables a reduction in gate length and therefore provides a semiconductor device of higher integration which is operable at a higher speed and substantially free from variations in finished size resulting from the use of different gate patterns." (see the abstract). Hence one of ordinary skill in the would have motivated to arrange the conductive useful structures and the conductive filler structure exhibit essentially the same height in order to make a uniform finished sizes of the gate electrode.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to have provided Shimomura et al. reference with

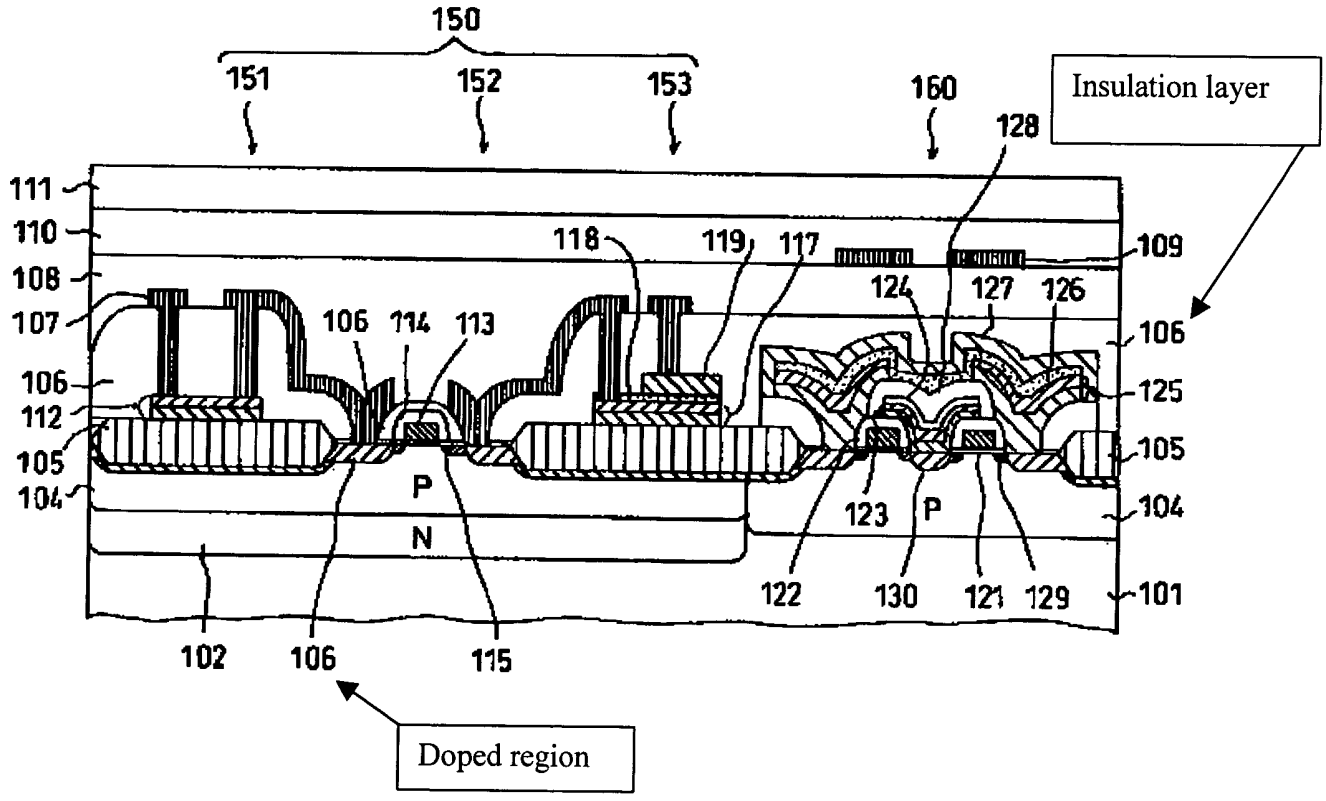
arranging the conductive useful structures and the conductive filler structure to exhibit essentially the same height as taught Uehara et al. because the arrangement would have provided the semiconductor device to have a uniform finished sizes of the gate electrode.

Response to Arguments

8. Applicants' arguments with respect to claims 11-21 have been considered but are moot in view of the new ground(s) of rejection.

Remarks

FIG.1



As shown above, in Fig. 1 of Shimomura et l. (US/5,736,421), both insulation layer and doped region labeled as **106.** However, the Examiner respectfully would like to point out the Applicants the two futures are given same reference number and should not be doubted that the existence of

"doped region" and "insulation layer" and the two are different in terms their material content and functions.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicants' disclosure Hsue et al. (US/5,521,113), Kim (US/5,714,410), Chen (US/5,731,234), and Kim (US/6,069,036) also disclose similar inventive subject matter.

Correspondence

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (703) 306-4511. The examiner can normally be reached on 8-5 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (703) 306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Brook Kebede
BK
May 2, 2003

W. David Coleman
Primary Examiner